

DATA SHEET

TDA8709A Video analog input interface

Product specification
Supersedes data of April 1993
File under Integrated Circuits, IC02

June 1994

Philips Semiconductors



PHILIPS

Video analog input interface

TDA8709A

FEATURES

- 8-bit resolution
- Sampling rate up to 32 MHz
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Low-level AC clock inputs and outputs
- Clamp function with selection for '16' or '128'
- No sample-and-hold circuit required
- Three selectable video inputs.

APPLICATIONS

- Video signal processing
- Digital picture processing
- Frame grabbing.
- Colour difference signals (U, V)
- R, G, B signals
- Chrominance signal (C).

GENERAL DESCRIPTION

The TDA8709A is an analog input interface for video signal processing. It includes a an input selector (one out-of-three video signals), video amplifier with clamp and external gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 32 MHz and an input selector.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{CCA}	analog supply voltage	4.5	5.0	5.5	V
V _{CCD}	digital supply voltage	4.5	5.0	5.5	V
V _{CCO}	TTL output supply voltage	4.2	5.0	5.5	V
I _{CCA}	analog supply current	–	40	47	mA
I _{CCD}	digital supply current	–	24	30	mA
I _{CCO}	TTL output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±0.5	LSB
f _{clk(max)}	maximum clock frequency	30	32	–	MHz
B	maximum –3 dB bandwidth (preamplifier)	12	18	–	MHz
P _{tot}	total power dissipation	–	380	512	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8709A	28	DIP	plastic	SOT117-1
TDA8709AT	28	SO28L	plastic	SOT136-1

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BLOCK DIAGRAM

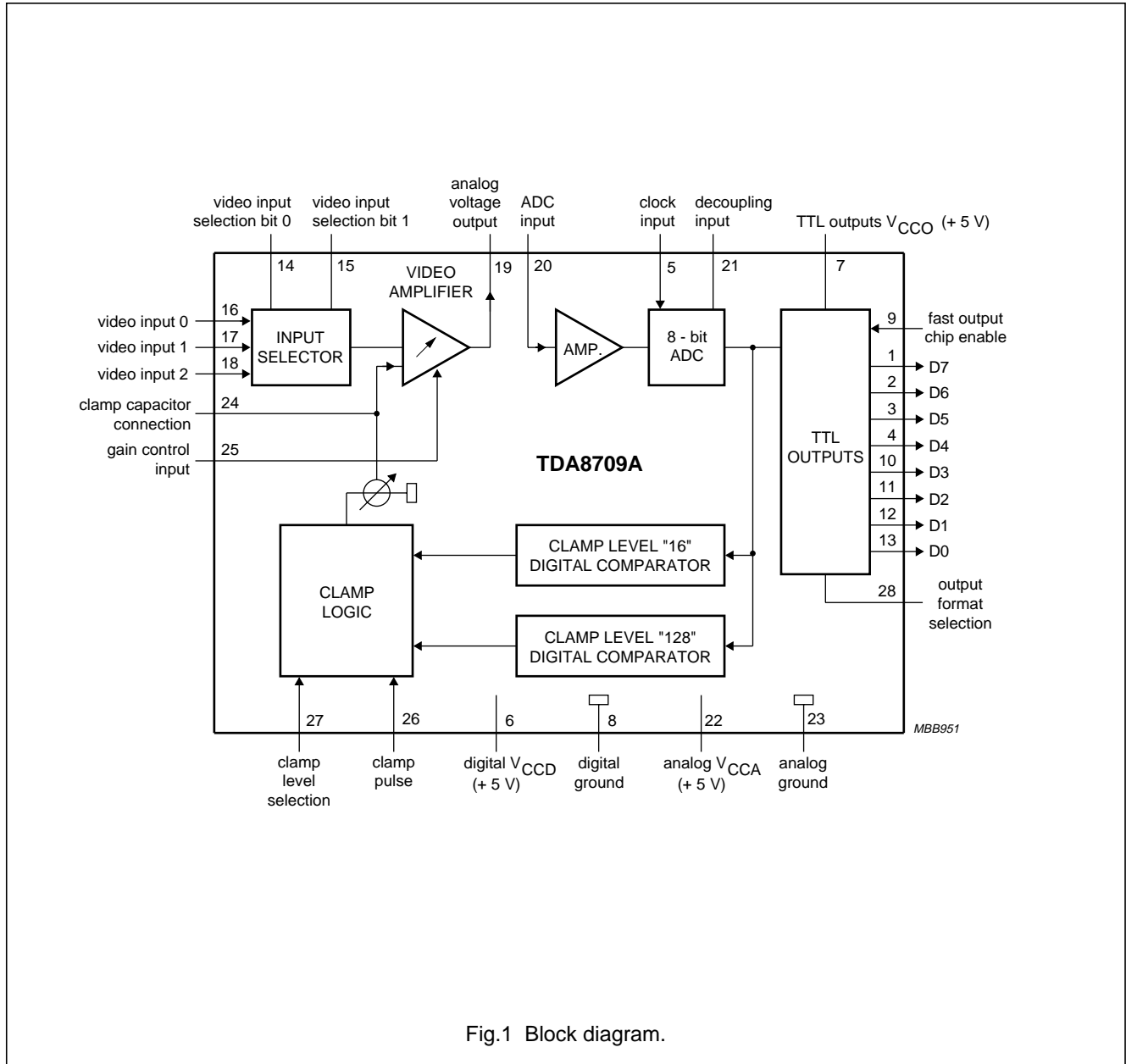


Fig.1 Block diagram.

Video analog input interface

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PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output; bit 7 (MSB)
D6	2	data output; bit 6
D5	3	data output; bit 5
D4	4	data output; bit 4
CLK	5	clock input
V _{CCD}	6	digital supply voltage (+5 V)
V _{CCO}	7	TTL outputs supply voltage (+5 V)
DGND	8	digital ground
FOEN	9	fast output chip enable
D3	10	data output; bit 3
D2	11	data output; bit 2
D1	12	data output; bit 1
D0	13	data output; bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V _{CCA}	22	analog supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
GAIN	25	gain control input
CLP	26	clamping pulse
CLS	27	clamping level selection input
OFS	28	output format selection

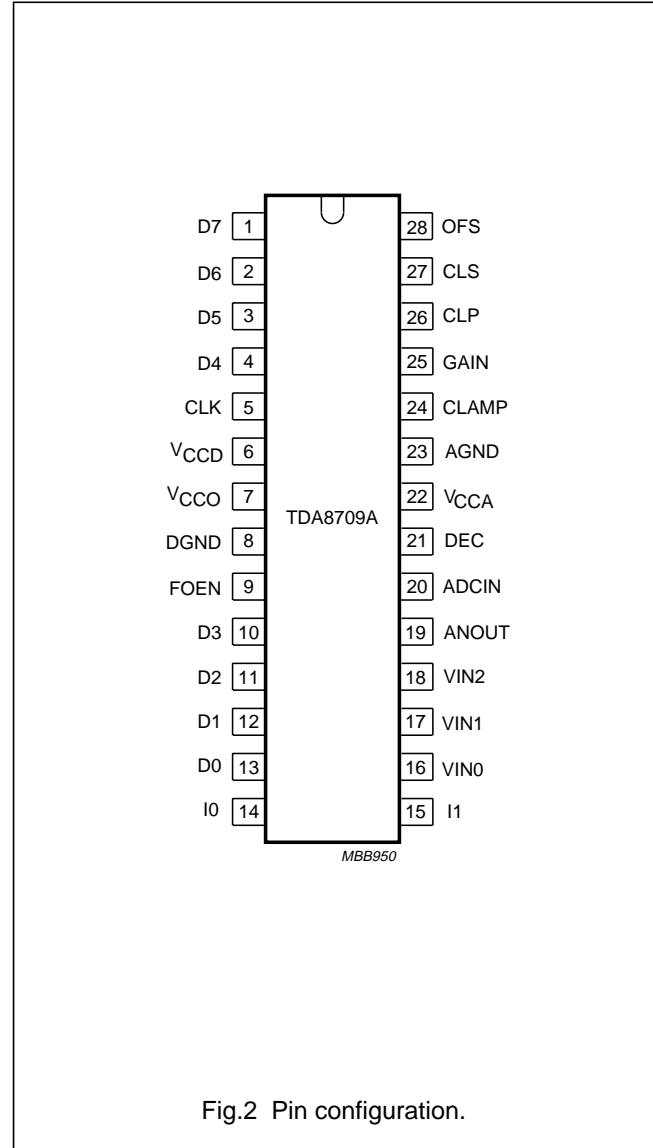


Fig.2 Pin configuration.

Video analog input interface

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FUNCTIONAL DESCRIPTION

TDA8709A is an 8-bit ADC with internal clamping and a preamplifier with adjustable gain.

The clamping value is switched via pin 27 between digital 16 (for R, G, B signals) and digital 128 (for

chrominance or colour difference signals). While clamping pulse at pin 27 is logic 1, the device will adjust the clamping level to the chosen value. The output format can be selected between binary and two's complement at pin 28.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	-0.3	+7.0	V
V_{CCD}	digital supply voltage	-0.3	+7.0	V
V_{CCO}	TTL output supply voltage	-0.3	+7.0	V
ΔV_{CC}	supply voltage difference between V_{CCA} and V_{CCD}	-0.5	+0.5	V
	supply voltage difference between V_{CCO} and V_{CCD}	-0.5	+0.5	V
	supply voltage difference between V_{CCA} and V_{CCO}	-1.0	+1.0	V
V_I	input voltage	-0.3	+7.0	V
I_O	output current	-	+10	mA
T_{stg}	storage temperature	-55	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
T_j	junction temperature	0	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air		
	SOT117-1	55	K/W
	SOT136-1	70	K/W

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CHARACTERISTICS

$V_{CCA} = V_{22}$ to $V_{23} = 4.5$ to 5.5 V; $V_{CCD} = V_6$ to $V_8 = 4.5$ to 5.5 V; $V_{CCO} = V_7$ to $V_8 = 4.2$ to 5.5 V; AGND and DGND shorted together; V_{CCA} to $V_{CCD} = -0.5$ to $+0.5$ V; V_{CCO} to $V_{CCD} = -0.5$ to $+0.5$ V; V_{CCA} to $V_{CCO} = -0.5$ to $+0.5$ V; $T_{amb} = 0$ to $+70$ °C; typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V and $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	40	47	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	TTL output supply current	TTL load (see Fig.7)	–	12	16	mA
Preamplifier inputs						
VIN0 TO VIN2 INPUTS						
$V_{I(p-p)}$	input voltage (peak-to-peak value)	note 1	0.6	–	1.5	V
$ Z_i $	input impedance	$f_i = 6$ MHz	10	20	–	k Ω
C_i	input capacitance	$f_i = 6$ MHz	–	1	–	pF
I0 AND I1 TTL INPUTS (SEE TABLE 1)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_I = 0.4$ V	–400	–	–	μ A
I_{IH}	HIGH level input current	$V_I = 2.7$ V	–	–	20	μ A
CLS, OFS AND CLP TTL INPUTS (SEE FIG.5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_I = 0.4$ V	–400	–	–	μ A
I_{IH}	HIGH level input current	$V_I = 2.7$ V	–	–	20	μ A
t_{CLP}	clamp pulse width		2	–	–	μ s
GAIN INPUT (PIN 25)						
$V_{25(min)}$	input voltage for minimum gain	see Fig.9	–	1.8	–	V
$V_{25(max)}$	input voltage for maximum gain	see Fig.9	–	3.8	–	V
I_I	input current		–	1.0	–	μ A
CLAMP INPUT (PIN 24)						
V_{24}	clamp voltage for code 128 output		–	3.5	–	V
I_{24}	clamp output current		see Table 2			

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video amplifier outputs						
ANOUT OUTPUT (PIN 19)						
$V_{19(p-p)}$	AC output voltage (peak-to-peak value)	$V_{OF} = 1.33 \text{ V (p-p)}$; $V_{25} = 3.0 \text{ V}$	–	1.33	–	V
I_{19}	internal current source	$R_L = \infty$	2.0	2.5	–	mA
$I_{O(p-p)}$	output current driven by the load	$V_{ANOUT} = 1.33 \text{ V (p-p)}$; note 2	–	–	1.0	mA
V_{19}	DC output voltage for black level	CLS = logic 1	–	$V_{CCA} - 2.02$	–	V
V_{19}	DC output voltage for black level	CLS = logic 0	–	$V_{CCA} - 2.6$	–	V
Z_{19}	output impedance		–	20	–	Ω
Preamplifier dynamic characteristics						
α_{ct}	crosstalk between VIN inputs	$V_{CCA} = 4.75 \text{ to } 5.25 \text{ V}$; note 3	–	–50	–45	dB
G_{diff}	differential gain	$V_{VIN} = 1.33 \text{ V (p-p)}$; $V_{25} = 3.0 \text{ V}$	–	2	–	%
ϕ_{diff}	differential phase	$V_{VIN} = 1.33 \text{ V (p-p)}$; $V_{25} = 3.0 \text{ V}$	–	0.8	–	deg
B	–3 dB bandwidth		12	–	–	MHz
S/N	signal-to-noise ratio	note 4	60	–	–	dB
SVRR1	supply voltage ripple rejection	note 5	–	45	–	dB
ΔG	gain range	see Fig.9	–4.5	–	+6.0	dB
G_{stab}	gain stability as a function of supply voltage and temperature	see Fig.9	–	–	5	%
Analog-to-digital converter inputs						
CLK INPUT (PIN 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_{clk} = 0.4 \text{ V}$	–400	–	–	μA
I_{IH}	HIGH level input current	$V_{clk} = 2.7 \text{ V}$	–	–	100	μA
$ Z_i $	input impedance	$f_{clk} = 10 \text{ MHz}$	–	4	–	$\text{k}\Omega$
C_i	input capacitance	$f_{clk} = 10 \text{ MHz}$	–	4.5	–	pF
FOEN INPUT (SEE TABLE 3)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_g = 0.4 \text{ V}$	–400	–	–	μA
I_{IH}	HIGH level input current	$V_g = 2.7 \text{ V}$	–	–	20	μA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADCIN INPUT (PIN 20; SEE TABLE 4)						
V ₂₀	input voltage	digital output = 00	–	V _{CCA} – 2.52	–	V
V ₂₀	input voltage	digital output = 255	–	V _{CCA} – 1.52	–	V
V _{20(p-p)}	input voltage amplitude (peak-to-peak value)		–	1.0	–	V
I ₂₀	input current		–	1.0	10	μA
Z _i	input impedance	f _i = 6 MHz	–	50	–	MΩ
C ₁	input capacitance	f _i = 6 MHz	–	1	–	pF
Analog-to-digital converter outputs						
DIGITAL OUTPUTS D0 TO D7						
V _{OL}	LOW level output voltage	I _{OL} = 2 mA	0	–	0.6	V
V _{OH}	HIGH level output voltage	I _{OL} = –0.4 mA	2.4	–	V _{CCD}	V
I _{OZ}	output current in 3-state mode	0.4 V < V _O < V _{CCD}	–20	–	+20	μA
Switching characteristics						
f _{clk(max)}	maximum clock input frequency	see Fig.5; note 6	30	32	–	MHz
Analog signal processing (f_{clk} = 32 MHz; see Fig.7)						
G _{diff}	differential gain	V ₂₀ = 1.0 V (p-p); see Fig.6; note 7	–	2	–	%
Φ _{diff}	differential phase	see Fig.6; note 7	–	2	–	deg
f ₁	fundamental harmonics (full-scale)	f _i = 4.43 MHz; note 7	–	–	0	dB
f _{all}	harmonics (full-scale); all components	f _i = 4.43 MHz; note 7	–	–55	–	dB
SVRR2	supply voltage ripple rejection	note 8	–	1	5	%/V
Transfer function						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 9	–	–	±2	LSB
Timing (f_{clk} = 32 MHz; see Figs 5, 6 and 7)						
DIGITAL OUTPUTS (C _L = 15 pF; I _{OL} = 2 mA; R _L = 2 kΩ)						
t _{ds}	sampling delay time		–	2	–	ns
t _h	output hold time		–	8	–	ns
t _d	output delay time		–	16	20	ns
t _{dEZ}	3-state delay time; output enable		–	16	25	ns
t _{dDZ}	3-state delay time; output disable		–	12	25	ns

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Notes to the “Characteristics”

1. 0 dB is obtained at the AGC amplifier when applying $V_{i(p-p)} = 1.33$ V.
2. The output current at pin 19 should not exceed 1 mA. The load impedance R_L should be referenced to V_{CCA} and defined as:
 - a) AC impedance ≥ 1 k Ω and the DC impedance > 2.7 k Ω .
 - b) The load impedance should be coupled directly to the output of the amplifier so that the DC voltage supplied by the clamp is not disturbed.
3. Input signals with the same amplitude. Gain is adjusted to obtain $ANOUT = 1.33$ V (p-p).

4. Signal-to-noise ratio measured with 5 MHz bandwidth:

$$\frac{S}{N} = 20 \log \frac{V_{ANOUT(p-p)}}{V_{ANOUT(RMS\ noise)}} \text{ at } B = 5 \text{ MHz.}$$

5. The voltage ratio is expressed as:

$$SVRR1 = 20 \log \frac{\Delta V_{CCA}}{V_{CCA}} \times \frac{G}{\Delta G} \text{ for } V_I = 1 \text{ V (p-p), gain at 100 kHz} = 1 \text{ and 1 V supply variation.}$$

6. It is recommended that the rise and fall times of the clock are ≥ 2 ns. In addition, a ‘good layout’ for the digital and analog grounds is recommended.
7. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
8. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

$$SVRR2 = \frac{\Delta (V_{I(00)} - V_{I(FF)}) + (V_{I(00)} - V_{I(FF)})}{\Delta V_{CCA}}$$

9. Full-scale sine wave ($f_i = 4.4$ MHz; $f_{clk} = 27$ MHz).

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Table 1 Video input selection (CVBS).

I1	I0	SELECTED INPUT
0	0	VIN0
0	1	VIN1
1	0	VIN2
1	1	VIN1

Table 3 FOEN input coding.

FOEN	D0 TO D7
0	active, two's complement
1	high impedance

Table 2 CLAMP output current.

CLS	CLP	DIGITAL OUTPUT	I _{CLAMP}
1	1	output < 128	+50 μA
		output > 128	-50 μA
X ⁽¹⁾	0	X	0 μA
0	1	output < 16	+50 μA
		16 < output	-50 μA

Note

1. X = don't care.

Table 4 Output coding and input voltage (typical values).

STEP	V _{ADCIN}	BINARY OUTPUTS								TWO'S COMPLEMENT							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Underflow	-	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V _{CCA} - 2.52 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	-	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.	-
.	-
254	-	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V _{CCA} - 1.52 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
Overflow	-	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

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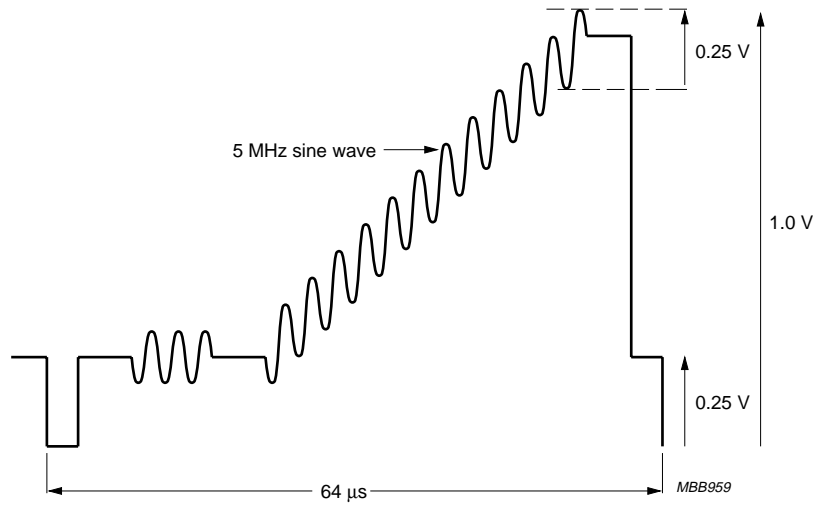


Fig.3 Test signal on the ADCIN pin for differential gain and phase measurements.

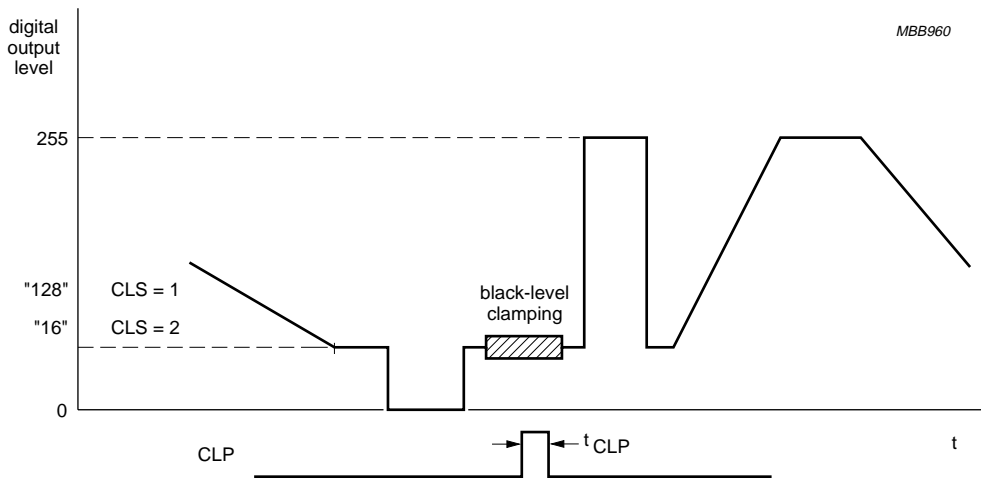


Fig.4 Control mode selection.

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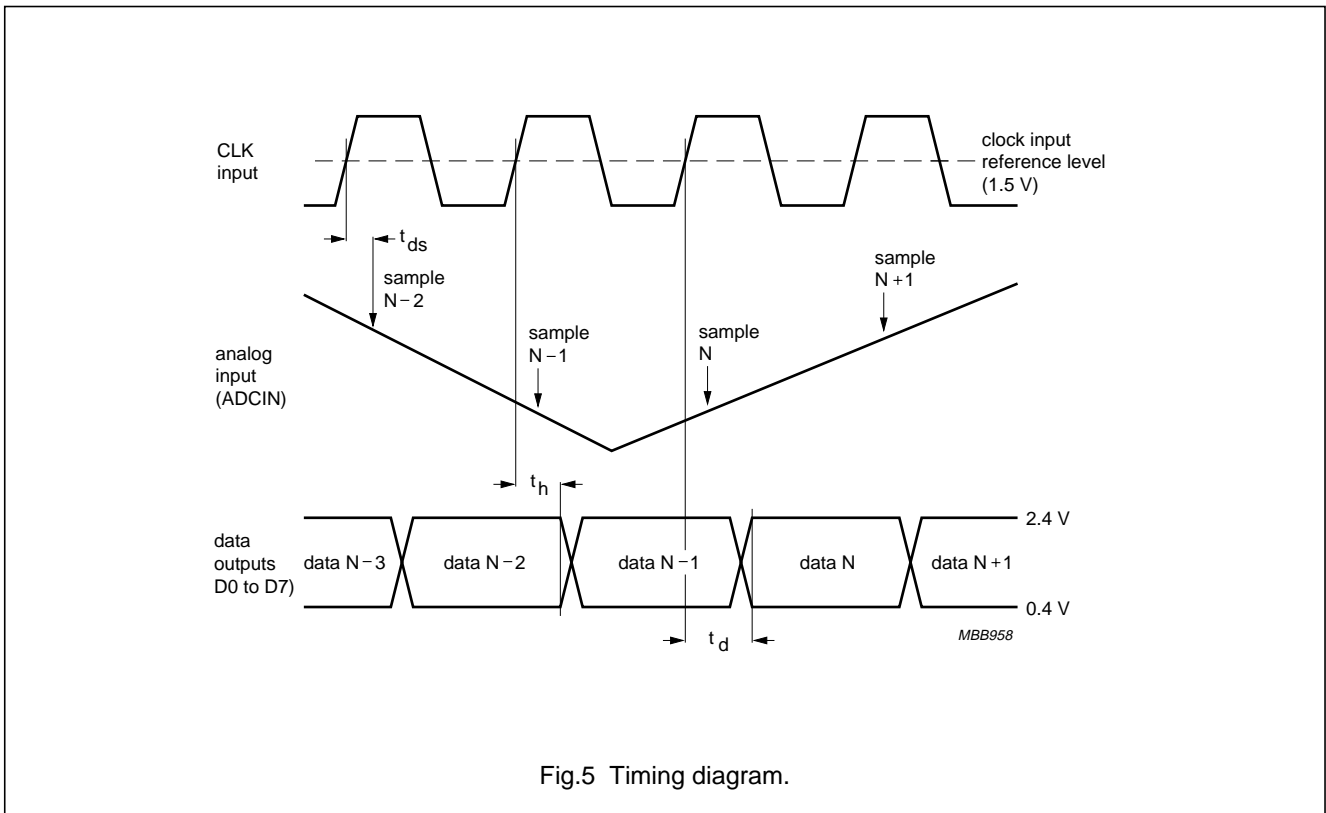


Fig.5 Timing diagram.

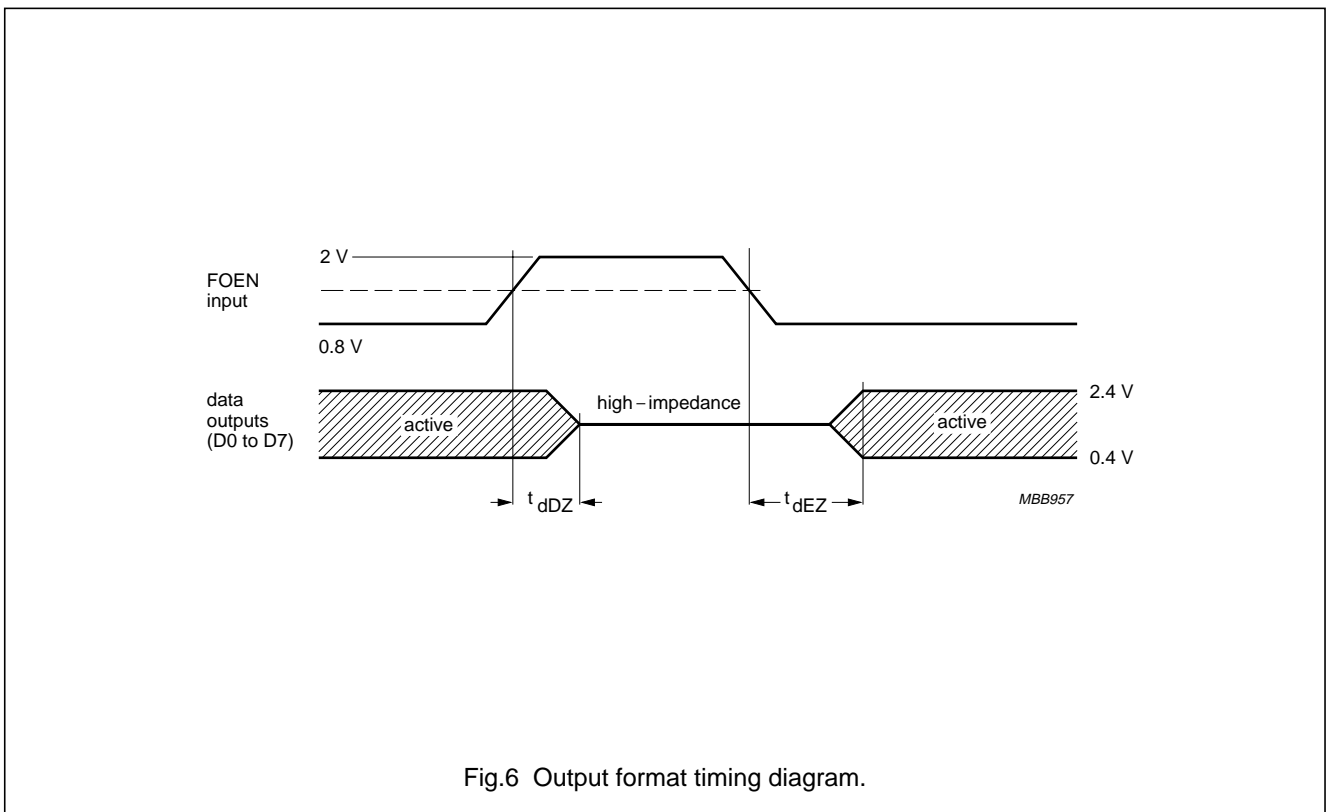


Fig.6 Output format timing diagram.

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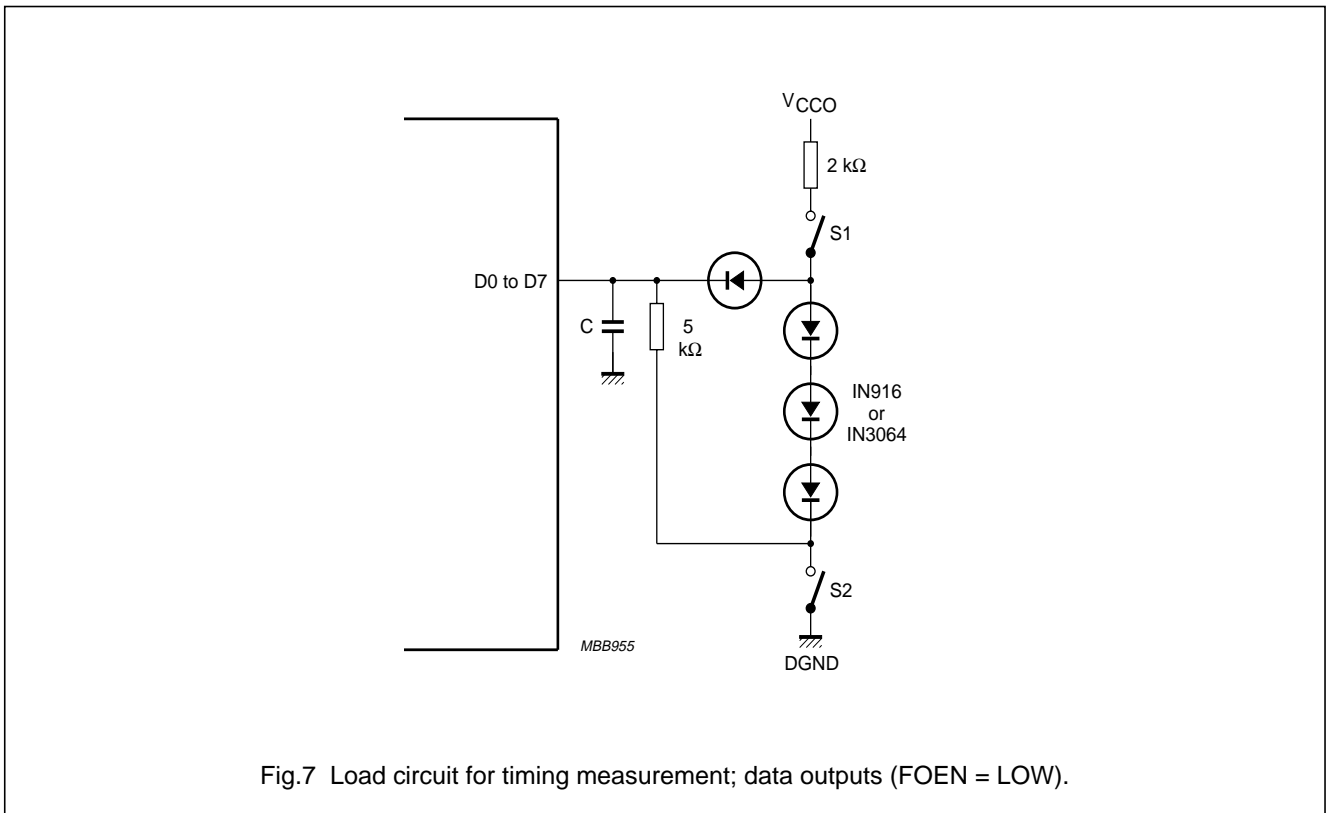


Fig.7 Load circuit for timing measurement; data outputs (FOEN = LOW).

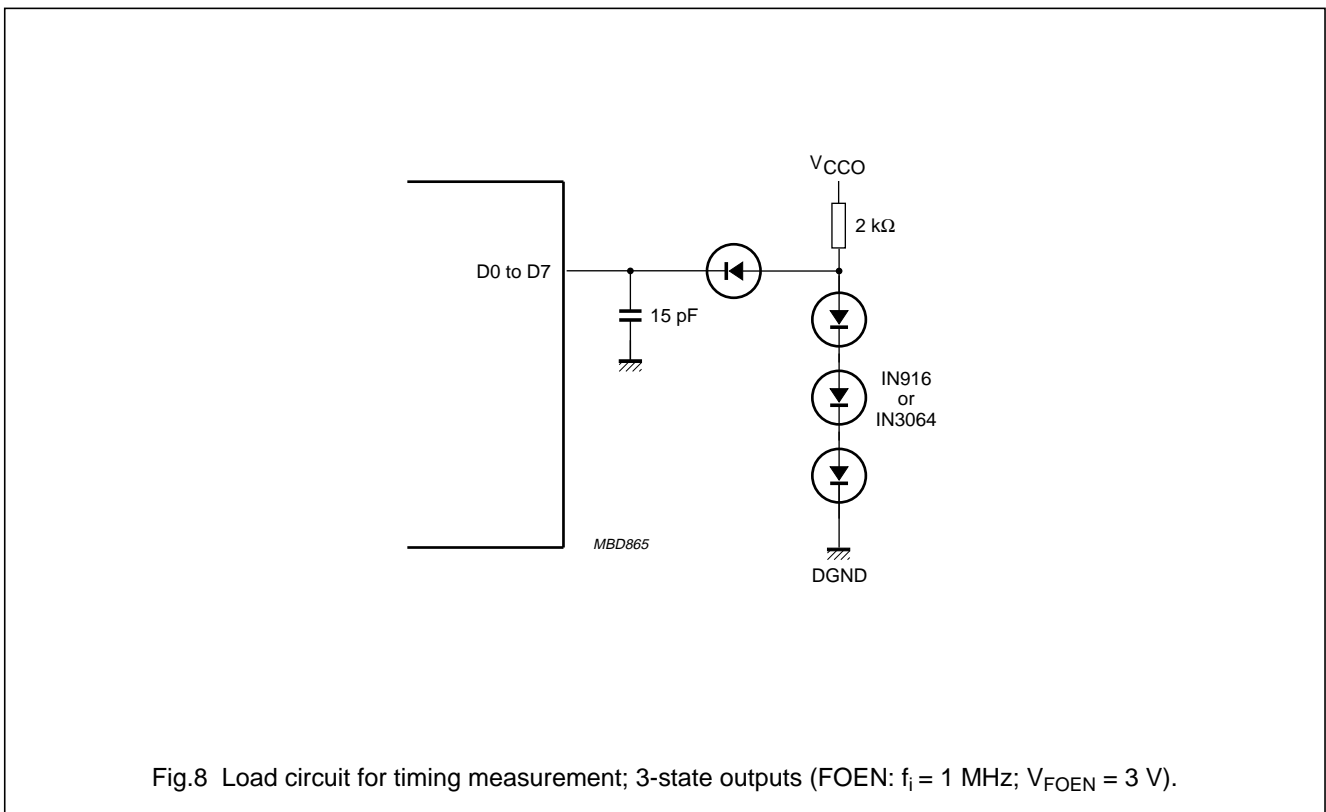
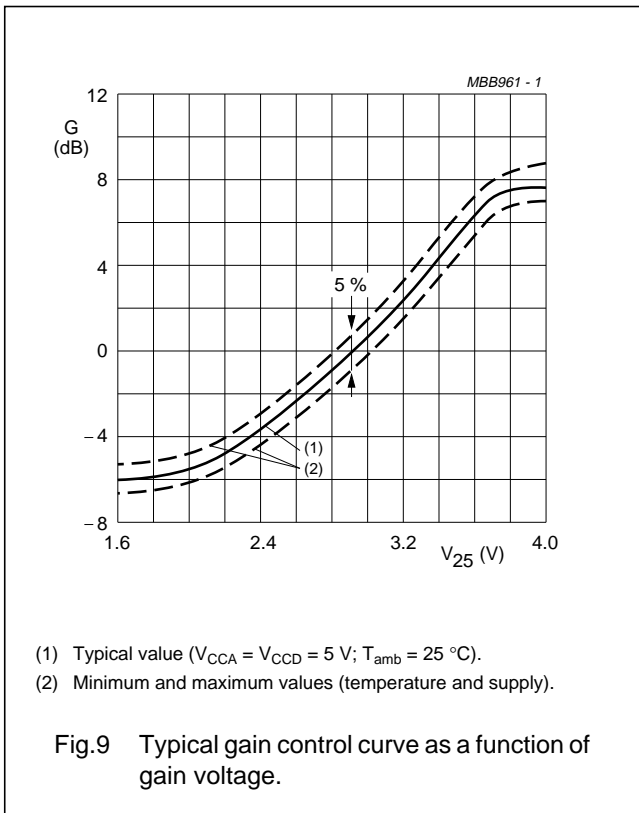


Fig.8 Load circuit for timing measurement; 3-state outputs (FOEN: $f_i = 1 \text{ MHz}$; $V_{FOEN} = 3 \text{ V}$).

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INTERNAL PIN CIRCUITRY

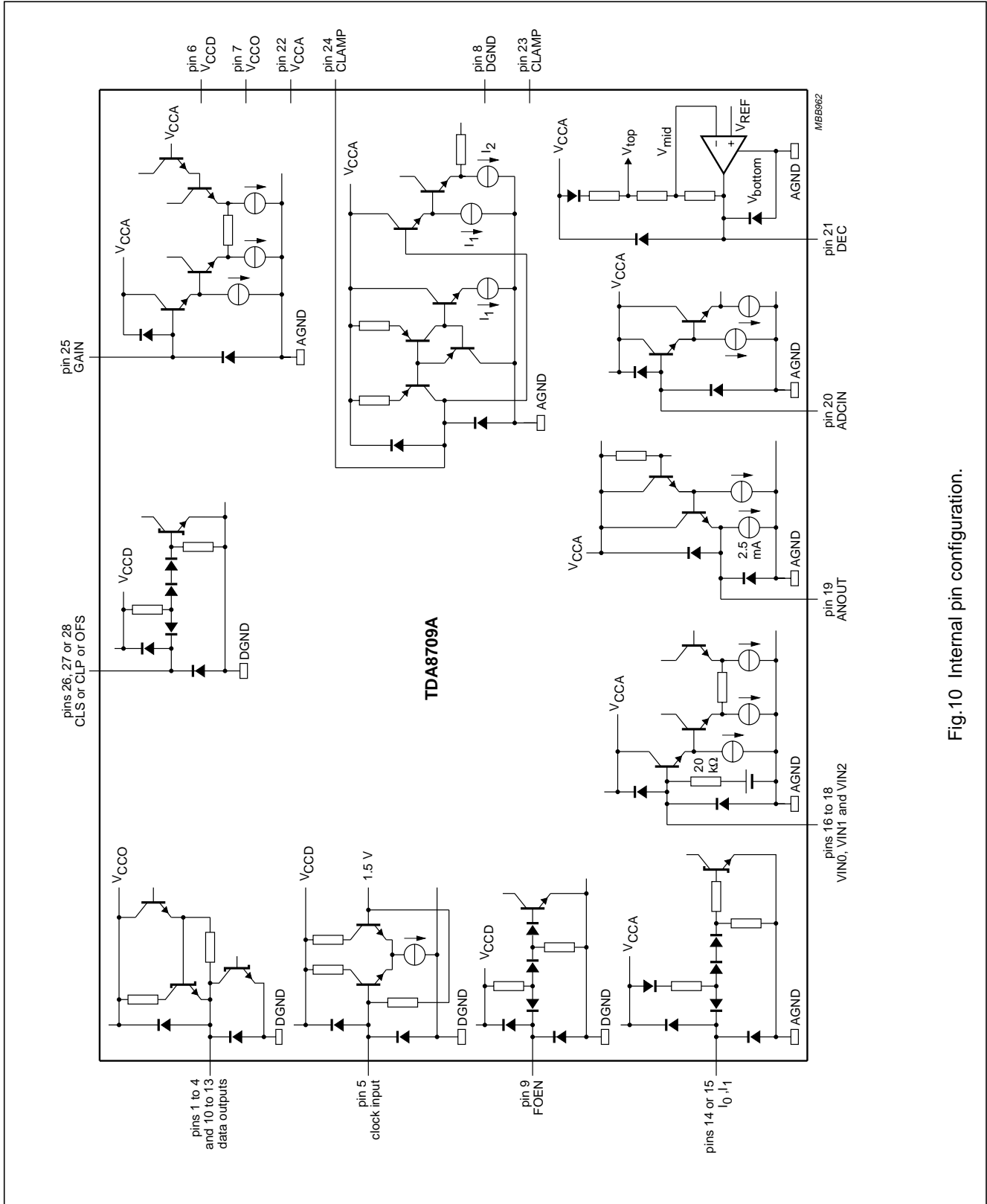


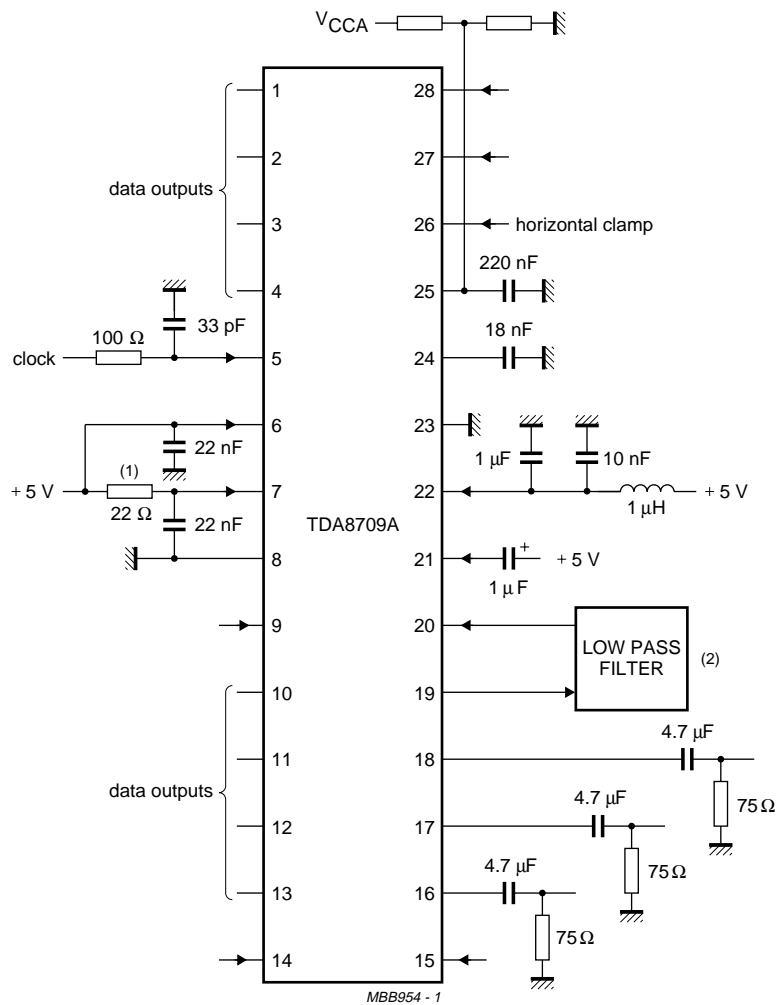
Fig.10 Internal pin configuration.

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APPLICATION INFORMATION

Additional information can be found in the laboratory report of TDA8708A "FBL/AN9308".

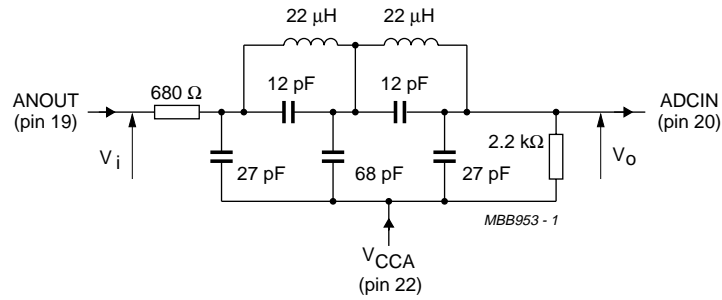


- (1) It is recommended to decouple V_{CC0} through a 22 Ω resistor especially when the output data of TDA8709A interfaces with a capacitive CMOS load device.
- (2) See Figs 12, 14, 16 and 18 for examples of the low-pass filters.

Fig.11 Application diagram.

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This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.12 Example of a low-pass filter for RGB and C signals.

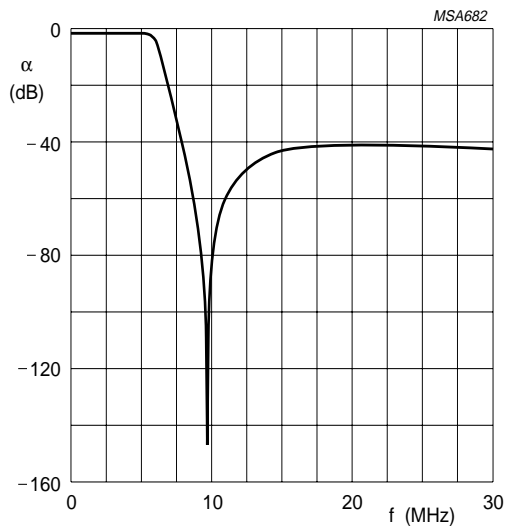


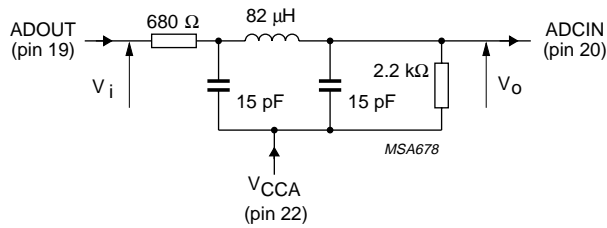
Fig.13 Frequency response for filter shown in Fig.12.

Characteristics of Fig.13

- Order 5; adapted CHEBYSHEV
- Ripple $p \leq 0.4$ dB
- $f = 6.5$ MHz at -3 dB
- $f_{\text{notch}} = 9.65$ MHz.

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This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.14 Example of an economical low-pass filter for RGB and C signals.

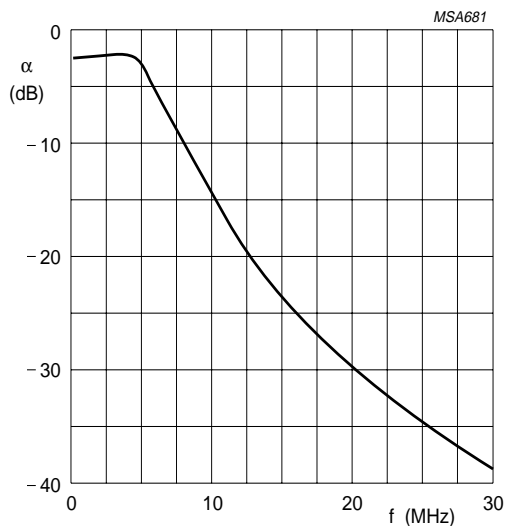


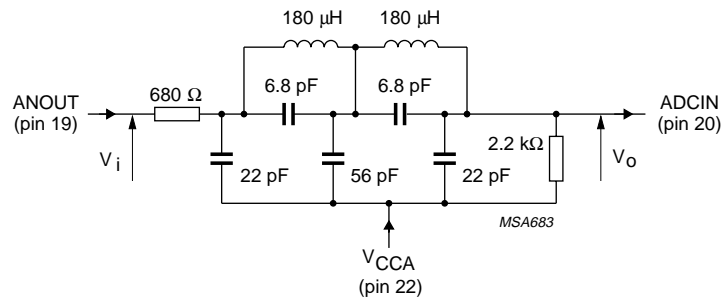
Fig.15 Frequency response for filter shown in Fig.14.

Characteristics of Fig.15

- Order 3; adapted CHEBYSHEV
- Ripple $p \leq 0.4$ dB
- $f = 6.5$ MHz at -3 dB.

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This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.16 Example of a low-pass filter for U and V signals.

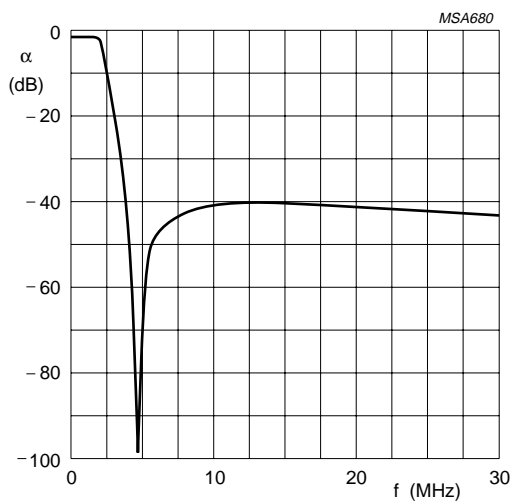


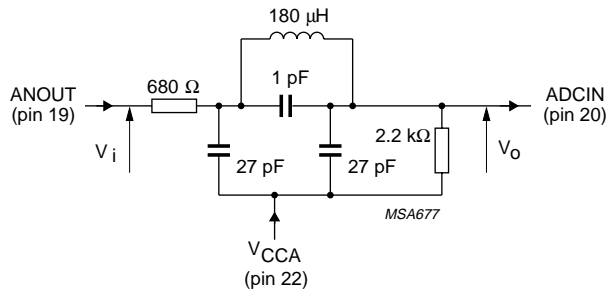
Fig.17 Frequency response for filter shown in Fig.16.

Characteristics of Fig.17

- Order 5; adapted CHEBYSHEV
- Ripple $p \leq 0.4$ dB
- $f = 2.3$ MHz at -3 dB
- $f_{\text{notch}} = 4.5$ MHz.

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This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.18 Example of an economical low-pass filter for U and V signals.

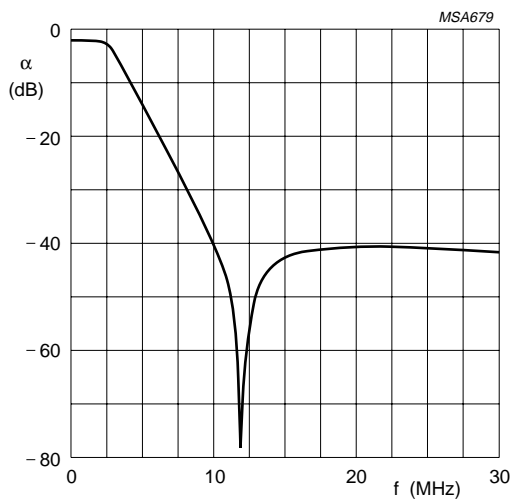


Fig.19 Frequency response for filter shown in Fig.18.

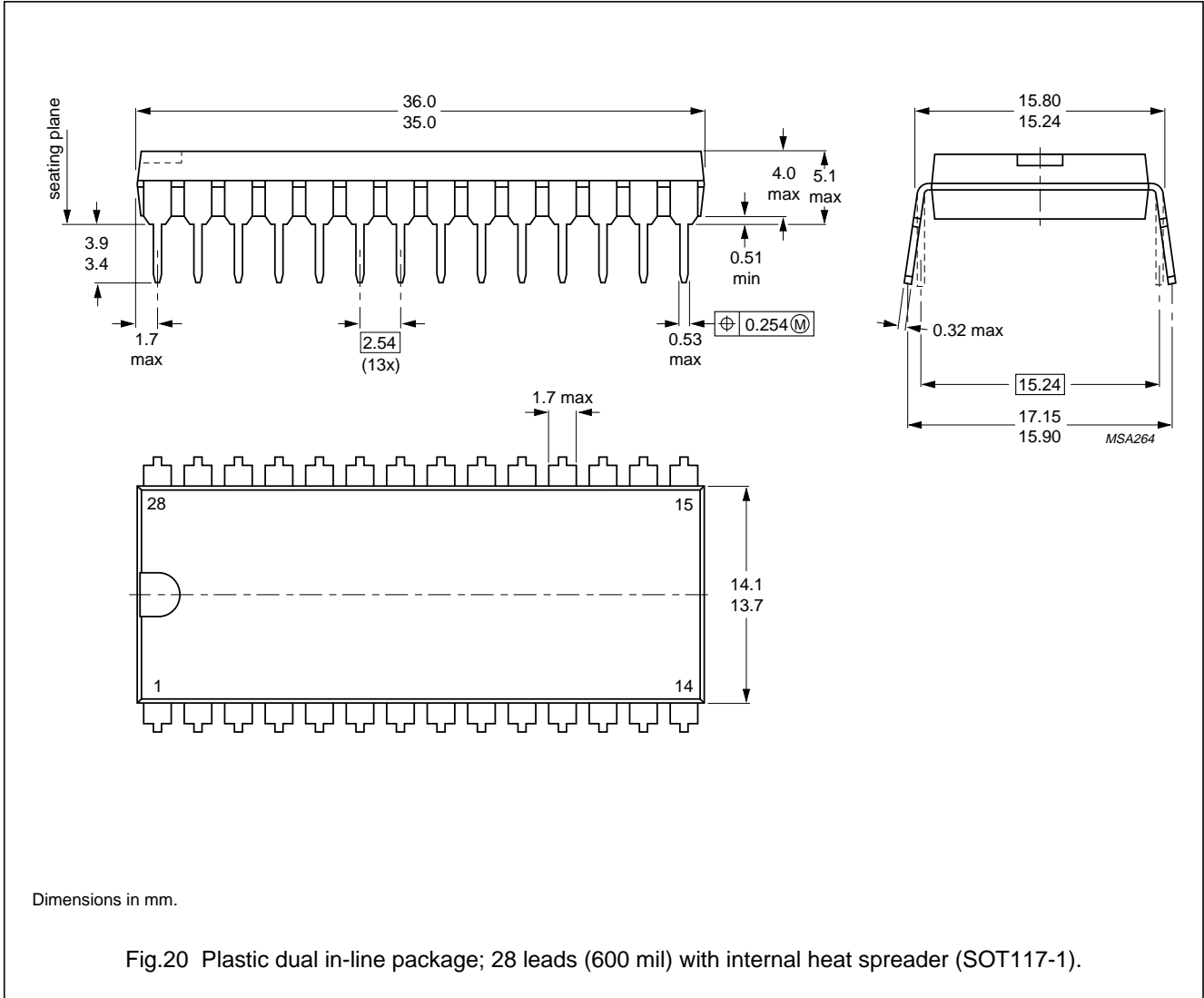
Characteristics of Fig.19

- Order 3; adapted CHEBYSHEV
- Ripple $p \leq 0.3$ dB
- $f = 2.8$ MHz at -3 dB
- $f_{\text{notch}} = 11.9$ MHz.

Video analog input interface

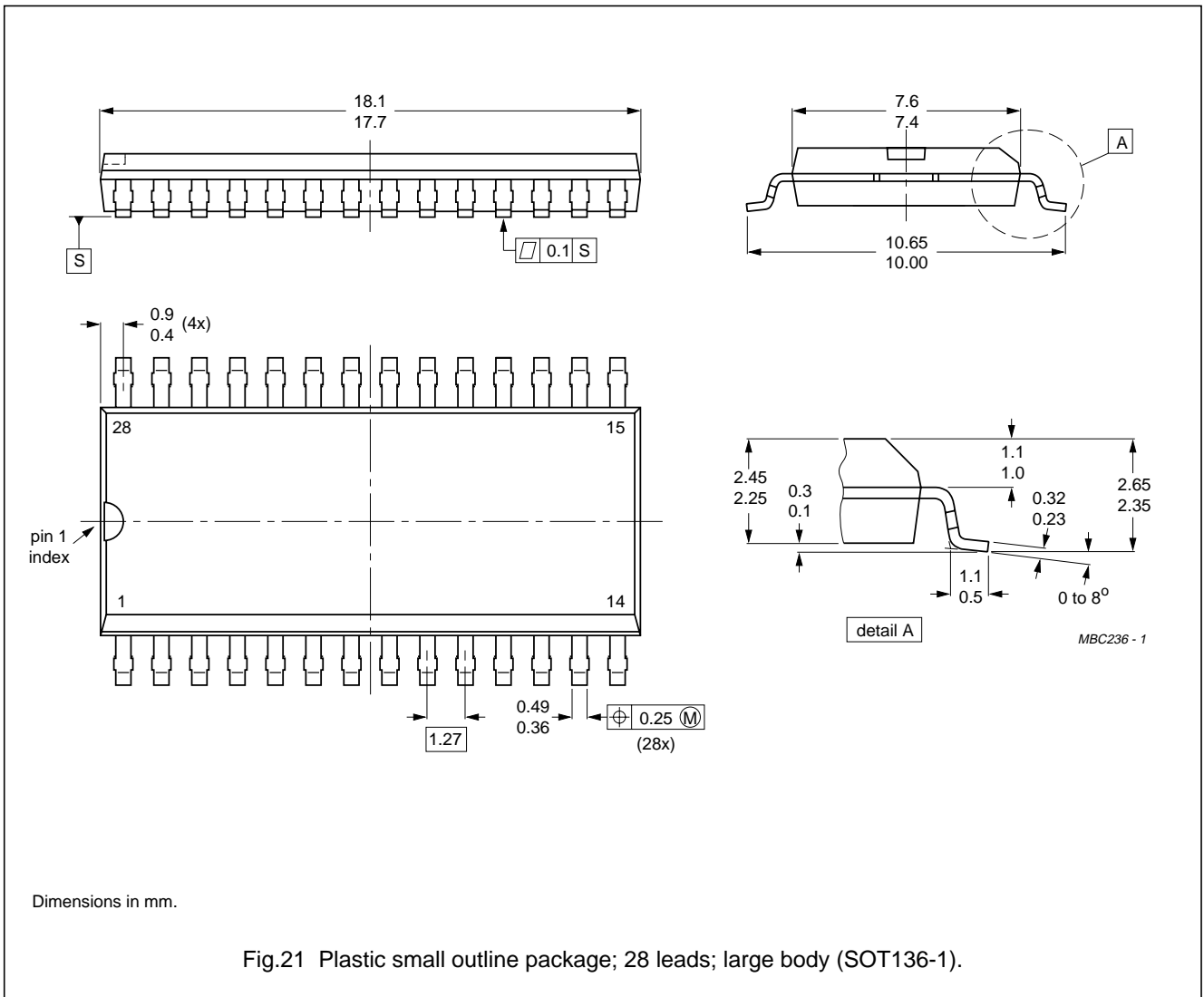
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PACKAGE OUTLINES



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SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

Plastic small-outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

Video analog input interface

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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Philips Semiconductors – a worldwide company

Argentina: IEROD, Av. Juramento 1992 - 14.b, (1428)
BUENOS AIRES, Tel. (541)786 7633, Fax. (541)786 9367

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. (02)805 4455, Fax. (02)805 4466

Austria: Triester Str. 64, A-1101 WIEN, P.O. Box 213,
Tel. (01)60 101-1236, Fax. (01)60 101-1211

Belgium: Postbus 90050, 5600 PB EINDHOVEN, The Netherlands,
Tel. (31)40 783 749, Fax. (31)40 788 399

Brazil: Rua do Rocio 220 - 5th floor, Suite 51,
CEP: 04552-903-SÃO PAULO-SP, Brazil.
P.O. Box 7383 (01064-970).

Tel. (011)821-2327, Fax. (011)829-1849

Canada: INTEGRATED CIRCUITS:

Tel. (800)234-7381, Fax. (708)296-8556
DISCRETE SEMICONDUCTORS: 601 Milner Ave,
SCARBOROUGH, ONTARIO, M1B 1M8,
Tel. (416)292 5161 ext. 2336, Fax. (416)292 4477

Chile: Av. Santa Maria 0760, SANTIAGO,
Tel. (02)773 816, Fax. (02)777 6730

Colombia: IPRELENZO LTDA, Carrera 21 No. 56-17,
77621 BOGOTA, Tel. (571)249 7624/(571)217 4609,
Fax. (571)217 4549

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. (032)88 2636, Fax. (031)57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. (9)0-50261, Fax. (9)0-520971

France: 4 Rue du Port-aux-Vins, BP317,
92156 SURESNES Cedex,
Tel. (01)4099 6161, Fax. (01)4099 6427

Germany: PHILIPS COMPONENTS UB der Philips G.m.b.H.,
P.O. Box 10 63 23, 20043 HAMBURG,
Tel. (040)3296-0, Fax. (040)3296 213.

Greece: No. 15, 25th March Street, GR 17778 TAVROS,
Tel. (01)4894 339/4894 911, Fax. (01)4814 240

Hong Kong: PHILIPS HONG KONG Ltd., Components Div.,
6/F Philips Ind. Bldg., 24-28 Kung Yip St., KWAI CHUNG, N.T.,
Tel. (852)424 5121, Fax. (852)428 6729

India: Philips INDIA Ltd, Components Dept,
Shivsagar Estate, A Block,
Dr. Annie Besant Rd. Worli, Bombay 400 018
Tel. (022)4938 541, Fax. (022)4938 722

Indonesia: Philips House, Jalan H.R. Rasuna Said Kav. 3-4,
P.O. Box 4252, JAKARTA 12950,
Tel. (021)5201 122, Fax. (021)5205 189

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. (01)640 000, Fax. (01)640 200

Italy: PHILIPS COMPONENTS S.r.l.,
Viale F. Testi, 327, 20162 MILANO,
Tel. (02)6752.3302, Fax. (02)6752 3300.

Japan: Philips Bldg 13-37, Kohnan2-chome, Minato-ku, TOKYO 108,
Tel. (03)3740 5028, Fax. (03)3740 0580

Korea: (Republic of) Philips House, 260-199 Itaewon-dong,
Yongsan-ku, SEOUL, Tel. (02)794-5011, Fax. (02)798-8022

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA,
SELANGOR, Tel. (03)750 5214, Fax. (03)757 4880

Mexico: Philips Components, 5900 Gateway East, Suite 200,
EL PASO, TX 79905, Tel. 9-5(800)234-7381, Fax. (708)296-8556

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB
Tel. (040)783749, Fax. (040)788399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. (09)849-4160, Fax. (09)849-7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. (022)74 8000, Fax. (022)74 8341

Pakistan: Philips Electrical Industries of Pakistan Ltd.,
Exchange Bldg. ST-2/A, Block 9, KDA Scheme 5, Clifton,
KARACHI 75600, Tel. (021)587 4641-49,
Fax. (021)577035/5874546.

Philippines: PHILIPS SEMICONDUCTORS PHILIPPINES Inc,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. (02)810 0161, Fax. (02)817 3474

Portugal: PHILIPS PORTUGUESA, S.A.,
Rua dr. António Loureiro Borges 5, Arquiparque - Miraflores,
Apartado 300, 2795 LINDA-A-VELHA,
Tel. (01)14163160/4163333, Fax. (01)14163174/4163366.

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. (65)350 2000, Fax. (65)251 6500

South Africa: S.A. PHILIPS Pty Ltd., Components Division,
195-215 Main Road Martindale, 2092 JOHANNESBURG,
P.O. Box 7430 Johannesburg 2000,
Tel. (011)470-5911, Fax. (011)470-5494.

Spain: Balmes 22, 08007 BARCELONA,
Tel. (03)301 6312, Fax. (03)301 42 43

Sweden: Kottbygatan 7, Akalla. S-164 85 STOCKHOLM,
Tel. (0)8-632 2000, Fax. (0)8-632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. (01)488 2211, Fax. (01)481 77 30

Taiwan: PHILIPS TAIWAN Ltd., 23-30F, 66, Chung Hsiao West
Road, Sec. 1. Taipei, Taiwan ROC, P.O. Box 22978,
TAIPEI 100, Tel. (02)388 7666, Fax. (02)382 4382.

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong,
Bangkok 10260, THAILAND,
Tel. (662)398-0141, Fax. (662)398-3319.

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. (0 212)279 2770, Fax. (0212)269 3094

United Kingdom: Philips Semiconductors Limited, P.O. Box 65,
Philips House, Torrington Place, LONDON, WC1E 7HD,
Tel. (071)436 41 44, Fax. (071)323 03 42

United States: INTEGRATED CIRCUITS:
811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. (800)234-7381, Fax. (708)296-8556
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P.O. Box 10330, RIVIERA BEACH, FLORIDA 33404,
Tel. (800)447-3762 and (407)881-3200, Fax. (407)881-3300

Uruguay: Coronel Mora 433, MONTEVIDEO,
Tel. (02)70-4044, Fax. (02)92 0601

For all other countries apply to: Philips Semiconductors,
International Marketing and Sales, Building BAF-1,
P.O. Box 218, 5600 MD, EINDHOVEN, The Netherlands,
Telex 35000 phtcnl, Fax. +31-40-724825

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